PhD Proposal 2017

School: Ecole Centrale de Lyon	
Laboratory: Lyon Institute of Nanotechnology	**Web site: http://inl.cnrs.fr**
Team: Heterogeneous Systems Design	**Head of the team: Ian O'Connor**
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Collaboration with other partner during this PhD: **In France:**	**In China:**

Title: Graphene Fe-FET Logic in Memory Computing
Scientific field: nanoelectronics, computing
Key words: logic in memory, graphene, Fe-FET, computing architecture, electronics

Details for the subject:

Background, Context:
As transistor scaling slows, emerging technologies and non-Von-Neumann computing paradigms are expected to take computing performance beyond conventional limits. Sustained progress in nanoelectronics now allows the integration of heterogeneous devices such as graphene FeFETs on CMOS. As a dense, high-speed, low-subthreshold slope and non-volatile device, the graphene Fe-FET can be considered to be the "ultimate" logic and storage device, beyond the limits of CMOS and intrinsically easier to integrate than other state-of-the-art proposals using magnetic or resistive devices (MTJs, RRAMs). The objective of the PhD is to propose and evaluate novel computing architectures relying on graphene Fe-FETs and to focus on the simulation and the programming of these architectures.

Research subject, work plan:
The Heterogeneous Systems Design group at INL has research interests in the modeling and simulation of computing hardware based on emerging technologies, while those of the Heteroepitaxy and Nanostructures group include the design and characterization of Fe-FET and graphene devices. The objective of the proposed PhD thesis is to exploit the logic and memory capabilities of graphene Fe-FET devices in order to propose highly efficient computing architectures.

The work is divided into the following successive steps:

- **compact modeling:** the main characteristics of graphene Fe-FET devices under development in the Heteroepitaxy and Nanostructures group will be extracted in order to develop a compact device model to enable logic and memory circuit design.
- **logic and memory circuit design:** the compact model will be used to explore logic and memory gate structures, and to predictively evaluate the performance levels of the circuits. The designed circuits will be fabricated by the Heteroepitaxy and Nanostructures group to compare predicted to measurement performance levels.
- **computing architecture studies:** the PhD candidate will examine novel compact non-volatile logic-in-memory architectures based on graphene FeFETs. In such architectures, storage elements are distributed in close proximity to a logic-circuit plane such that storage and logic are merged, global wirelength (and consequently dynamic power) is reduced, and (due to the non-volatile characteristics of the memory) leakage power can also be eliminated. It will be necessary to build system-level architecture models in the SystemC language and to carry out estimations of average and peak instruction execution speed, energy consumption profiling and long-term reliability.

References:

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[2] N. Yakymets, I. O'Connor, K. Jabeur, S. Le Beux, "Multi-Level Mapping of Nanocomputer Architectures Based on Hardware Reuse," IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), Special Issue on Computing in Emerging Technologies, vol. 5, no. 1, pp. 88-97, Mar. 2015

[3] G. Niu, S. Yin, G. Saint-Girons, B. Gautier, P. Lecoeur, V. Pillard, G. Hollinger, B. Vilquin, "Epitaxy of BaTiO3 thin film on Si(0 0 1) using a SrTiO3 buffer layer for non-volatile memory application", Microelectronics Engineering 88, 1232 (2011).